WHAT IS CLAIMED IS:

1. A power-saving circuit for an active matrix liquid crystal display ("LCD") panel, comprising:

a plurality of first capacitors, each first capacitor corresponding to a data line of the LCD panel for collecting electrical charge provided on an associated data line;

at least one set of second capacitors;

at least one set of transistors, each transistor of a set corresponding to one of the plurality of first capacitors; and

at least two control signals, each control signal corresponding to a set of the at least one set of transistors and corresponding to a set of the at least one set of second capacitors, and each control signal functioning to switch between a first and a second state to control the operation state of an associated set of transistors,

wherein the at least two control signals switch to a first state in a first sequence starting from a first control signal to a last control signal, and then in a second sequence starting from the last control signal to the first control signal, the first sequence alternating with the second sequence.

2. The circuit of claim 1, wherein each second capacitor of a set in response to a first state of an associated control signal reaches a voltage level that is an average of a voltage level of the each second capacitor held at a previous first state of the associated control signal and a voltage level of an associated first capacitor in proportion to the capacitance values of the each second capacitor and the associated first capacitor.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

3. The circuit of claim 1, wherein each transistor includes a gate coupled to an associated control signal, a first terminal coupled to an associated first capacitor, and a second terminal coupled to an associated second capacitor.

4. The circuit of claim 3, wherein the second terminals of a subset of transistors of a set are coupled to a same second capacitor.

5. The circuit of claim 1, wherein each first capacitor includes a first capacitance value, and each second capacitor includes a second capacitance value substantially the same as the first capacitance value.

6. The circuit of claim 5, wherein the first and second capacitance values are predetermined.

7. The circuit of claim 1, wherein the at least two control signals include a first control signal and a second control signal, and a voltage level of one set of second capacitors associated with the first control signal swings between V_{COM} + 1/2 V_{LC} and V_{COM}, and a voltage level of the other set of second capacitors associated with the second control swings between V_{COM} and V_{COM} - 1/2 V_{LC}, where V_{COM} is a voltage applied to a common electrode of the LCD panel, and V_{LC} is a voltage difference between a pixel electrode and a common electrode of the LCD panel during a black-scale image.

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8. The circuit of claim 1, wherein a set of second capacitors is formed between a data driver and a cell matrix driven by the data driver of the LCD panel.

9. A power-saving circuit for an active matrix liquid crystal display ("LCD") panel, comprising:

a plurality of first capacitors, each first capacitor corresponding to a data line of the LCD panel for collecting electrical charge provided on an associated data line;

a plurality of second capacitors;

a plurality of transistors, each transistor including a gate, a first terminal coupled to one of the plurality of first capacitors, and a second terminal coupled to one of the plurality of second capacitors; and

a control signal coupled to the gates of the plurality of transistors, and functioning to switch between a first and a second state to control the operation state of the plurality of transistors,

wherein each second capacitor in response to a first state of the control signal reaches a voltage level that is an average of a voltage level of the each second capacitor held at a previous first state of the control signal and a voltage level of an associated first capacitor in proportion to the capacitance values of the each second capacitor and the associated first capacitor.

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10. The circuit of claim 9, wherein each first capacitor includes a first capacitance value, and each second capacitor includes a second capacitance value substantially the same as the first capacitance value.

11. The circuit of claim 10, wherein the first and second capacitance values are predetermined.

12. The circuit of claim 9, wherein the second terminals of a subset of the plurality of transistors are coupled to a same second capacitor.

13. The circuit of claim 9, wherein the number of the plurality of transistors is same as that of the plurality of second capacitors.

14. The circuit of claim 9, wherein the a voltage level of one of the second capacitors swings between V_{COM} + 1/3 V_{LC} and V_{COM} - 1/3 V_{LC}, where V_{COM} is a voltage applied to a common electrode of the LCD panel, and V_{LC} is a voltage difference between a pixel electrode and a common electrode of the LCD panel during a black-scale image.

15. A method of power saving for an active matrix liquid crystal display ("LCD") panel, comprising:

providing a plurality of first capacitors;

electrically coupling each first capacitor to a data line of the LCD panel;

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HENDERSON
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GARRETT &
DUNNER LLP

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Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

providing at least one set of transistors;

electrically coupling each transistor of a set to one of the plurality of first capacitors;

providing at least one set of second capacitors;

electrically coupling each set of second capacitors to a set of transistors;

providing at least one control signal;

electrically coupling each control signal to a set of transistors, each control signal functioning to switch between a first and a second state to control the operation state of an associated set of transistors;

switching the at least one control signal to a first state in a first sequence starting from a first control signal to a last control signal such that voltage levels of a second capacitor and an associated first capacitor are averaged in proportion to their respective capacitance values; and

switching the at least one control signal in a second sequence starting from the last control signal to the first control signal such that voltage levels of a second capacitor and an associated first capacitor are averaged in proportion to their respective capacitance values.

16. The method of claim 15, further comprising repeating the first and second sequences.

17. The method of claim 15, further comprising coupling a gate of each transistor of a set to an associated control signal, coupling a first terminal of the each

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DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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transistor of a set to an associated first capacitor, and coupling a second terminal of the each transistor of a set to an associated second capacitor.

18. The method of claim 15, further comprising coupling the second terminals of at least two transistors of a set to a same second capacitor.

19. The method of claim 15, wherein each first capacitor includes a first capacitance value, and each second capacitor includes a second capacitance value substantially the same as the first capacitance value.

20. The method of claim 15, wherein the at least one set of transistors includes amorphous or poly-crystalline thin film transistors.

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GARRETT &
DUNNER LLP

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Washington, DC 20005
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